

IAP4 Rec'd PCT/PTO 11 JAN 2006
PCT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: SASAO, Tsutomu, et al.

Group Art Unit: Not yet assigned

Serial No.: 10/551,391

Examiner: Not yet assigned

Filed: September 29, 2005

Confirmation No.: 3333

For: PROGRAMMABLE LOGIC DEVICE

INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 CFR 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

January 11, 2006

Sir:

The attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached Form PTO-1449. One copy of each of these documents, except for the U.S. publication, is attached.

References AE and AG were cited in an International Search Report and previously listed on a PTO Form 1449 filed September 29, 2005. A copy of the Search Report was also filed on September 29, 2005. References AA, AE and AF were discussed in the specification.

No fee or certification is required in connection with this Information Disclosure Statement, since it is being submitted prior to the issuance of a first official action on the merits or expiration of the three month period following the filing date or the entry of the national stage of the above-captioned application.

The above information is presented so that the Patent and Trademark Office can, in the first instance, determine any materiality thereof to the claimed invention. It is respectfully requested that

02 JAN 13 11:2:00



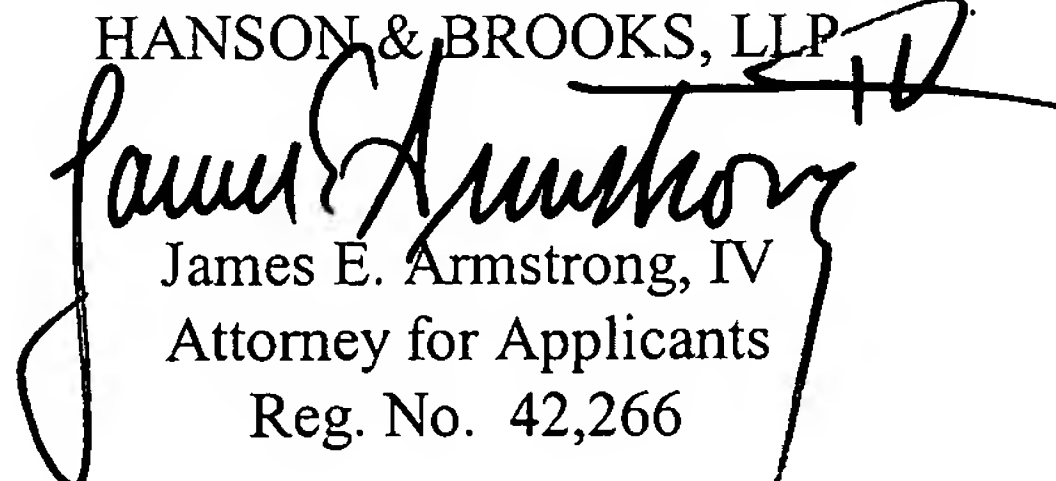
Serial No.: 10/551,391

the information be expressly considered during the prosecution of this application, and that the documents cited in the attached Form PTO-1449 be made of record therein and appear on the first page of any patent to issue therefrom.

The Commissioner is authorized to charge our Deposit Account No. 01-2340 for any fee which is deemed by the Patent and Trademark Office to be required to effect consideration of this statement.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS,
HANSON & BROOKS, LLP


James E. Armstrong, IV
Attorney for Applicants
Reg. No. 42,266

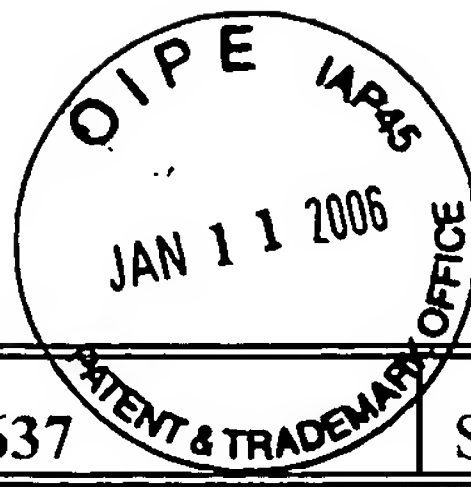
JAM/aoa
Atty. Docket No. 050637
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930



23850

PATENT TRADEMARK OFFICE

Enclosures: PTO-1449 and references (10)



INFORMATION DISCLOSURE CITATION PTO-1449	Atty. Docket No. 050637	Serial No. 10/551,391
	Applicant(s): SASAO, Tsutomu, et al.	
	Filing Date: September 29, 2005	Group Art Unit: Not yet assigned

U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
_____	AA	Re. 34,363	R. H. Freeman	08/31/1993			
_____	AB						

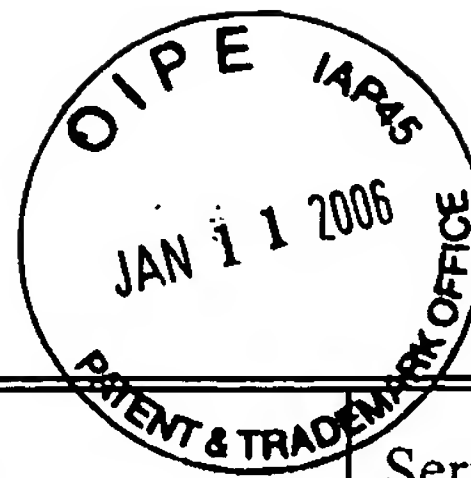
FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Translation (Yes or No)
_____	AC				
_____	AD				

OTHER DOCUMENTS

_____	AE	T. Sasao et al., "A Cascade Realization of Multiple-Output Function and Its Application to Reconfigurable Hardware," The Institute of Electronics, Information and Communication Engineers, Vol. 101, No. 3, Mie University, FTS2001-8, April 2001, pp. 57-64. English abstract is included. Discussed in the specification.
_____	AF	T. Sasao et al. "A Cascade Realization of Multiple-Output Function for Reconfigurable Hardware" International Workshop on Logic and Synthesis (IWLS01), Lake Tahoe, CA, June 12-15, 2001, pp. 225-230 w/cover page and the TOC, Discussed in the specification.
_____	AG	A. Tomita et al., "A Design of LUT-Array-Based PLD," The Institute of Electronics, Information and Communication Engineers, Vol. 100, No. 475, November 2000, pp. 173-178. English abstract is included.

Examiner	Date Considered
----------	-----------------



INFORMATION DISCLOSURE CITATION PTO-1449	Atty. Docket No. 050637	Serial No. 10/551,391
	Applicant(s): SASAO, Tsutomu, et al.	
	Filing Date: September 29, 2005	Group Art Unit: Not yet assigned

OTHER DOCUMENTS

_____	BA	Y. Iguchi et al., "Realization of Multiple-Output Functions by Reconfigurable Cascades, " International Conference on Computer Design :VLSI in Computers & Processors (ICCD-2001), Austin, TX, Sept. 23-26, 2001. pp. 388-393 (published page number).
_____	BB	A. Mishchenko et al., "Encoding of Boolean Functions and Its Application to LUT Cascade Synthesis, " International Workshop on Logic and Synthesis (IWLS2002), New Orleans, Louisiana, June 4-7, 2002, pp.115-120.
_____	BC	T. Sasao, "Design Methods for Multi-Rail Cascades," International Workshop on Boolean Problems (IWBP2002), Freiberg, Germany, Sept. 19-20, 2002, pp. 123-132.
_____	BD	T. Sasao et al., "A Design Method for Irredundant Cascades," International Symposium on New Paradigm VLSI Computing, Sendai, Japan, Dec. 12-14, 2002, pp.37-40.
_____	BE	A. Mishchenko et al., "Logic Synthesis of LUT Cascades with Limited Rails," The Institute of Electronics, Information and Communication Engineers, Lake Biwa, VLD2002-99, November 2002, pp. 1-6.
_____	BF	H. Gouji et al., "On a Method to Reduce the Number of LUTs in LUT cascades," The Institute of Electronics, Information and Communication Engineers, Kitakyushu, VLD2001-99, November 2001, 6 sheets, English abstract is included.
_____	BG	M. Matsuura et al., "Compact Representaions of BDDs for Multiple-Output Functions and Their Optimization," The Institute of Electronics, Information and Communication Engineers, Kitakyushu, VLS2001-100, November 2001, 6 sheets, English abstract is included.
Examiner	Date Considered	